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EXAMINER	
RODRIGUEZ, GLENDA P	

ART UNIT	PAPER NUMBER
2651	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,009	HEYDARI ET AL.	
	Examiner	Art Unit	
	Glenda P. Rodriguez	2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patapoutian et al. (US Patent No. 5, 661, 760) in view of Fredrickson et al. (US Patent No. 6, 400, 288).

Regarding Claims 1, 4, 8, 20, 24, 27, 32 and 33, Patapoutian et al. teaches a coded binary sequence, which has a first group bits that are consecutive, the first group having first and second portions both representing a first logic level, the bits in the first portion having a second logic level and the bits in the second portion having a third logic level (Pat. No. 5, 661, 760; Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "1011" ("10" being a first logic level and "11" being a second logic level) will be encoded into "--++++----++--++", having a first and second equally sized portion in the first group ("--++" and "++--") having a second logic level ("1") and a third logic level ("0") (The description of Patent Application is according to the instant specification, and, it is concurrent with Page 6, Table 1 to Page 7, Line 13 of the instant specification.).); and a second group of consecutive bits, the second group having first and second portions and representing a fourth logic level, the bits in the first portion having a fifth logic level and the bits in the second portion having a sixth logic level ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "-

-++") having a fourth logic level ("1") and a fifth logic level ("1"))(It would have been obvious for an artisan to know that the logiclevels could be either the same or different than their previous logic levels). Patapoutian et al. fail to teach wherein one of the groups is palindromic. However, this feature is well known in the art as disclosed by Fredrickson et al., wherein it teaches a sequence of 00001100, wherein one of the groups is palindromic ("0000") and the second group has a third logic level ("11") and a fourth logic level ("00") (Pat. No. 6, 400, 288; Table 3, wherein Fredrickson et al. teach a Table with different binary sequences.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to generate binary sequences in order to reduce the occurrence of bit shift errors (Pat. No. 6, 400, 288; Col. 10, Lines 43-48).

Claim 10 has limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 10 however also recites the following limitations: "disk sectors operable to store application data and servo wedges that store servo data" (Pat. No. 5, 661, 760; Col. 6, Lines 15-61 and Col. 6, Lines 15-61).

Claim 11 has limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 11 however also recites the following limitations: "a Viterbi detector" (Pat. No. 5, 661, 760; See Abstract).

Claim 14 has limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 14 however also recites the following limitations: "a sample circuit to generate samples of a signal" (Pat. No. 5, 661, 760; See Abstract).

Claim 16 has limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 14 however also recites the following limitations: "a

data storage disk having a surface, data sectors at respective locations of the surface, and servo wedges that store servo data, a motor, a read head and a read head positioning circuit and a servo circuit" (Pat. No. 5, 661, 760; Col. 5, Lines 15-21 and Col. 6, Lines 15-61, Servo data are used for non-application purposes).

Regarding Claim 2, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claim 1. Patapoutian et al. further teach wherein the first and second portions of the first group respectively comprise first and second halves of the first group (Pat. No. 5, 661, 760; Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that the first group with two portions (group "10") can be divided in to first and second halves: "10" or "--++++--" can be divided into "--++" and "++--".); and the first and second equally of the second group respectively comprise first and second halves of the second group ("11" would be the second group (fourth logic level) which also has two portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1")).

Regarding Claim 6, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claim 1. Patapoutian et al. further teach wherein the first and second groups each respectively comprise four consecutive bits (Patapoutian et al. teaches that each group of bits consists of 4 consecutive bits (Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--").).

Regarding Claim 7, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claim 4. Patapoutian et al. further teach the first and second portions of the second group respectively comprises first and second halves of the second group ("11" would be the second

group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1").).

Regarding Claim 12, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claim 11. Patapoutian et al. further teaches wherein the binary sequence comprises a coded binary sequence (Pat. No. 5, 661, 760; See Abstract).

Regarding Claim 13, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claim 11. Patapoutian et al. further teach wherein the first logic level comprises a logic 0; and the second logic level comprises a logic 1 (Pat. No. 5, 661, 760; Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "10" will be encoded into "--++++--", having a first and second equally sized portion in the first group ("--++" and "++--").).

Regarding Claim 15, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claim 14. Patapoutian et al. further teach a decoder coupled to the Viterbi detector and operable to decode the recovered binary sequence (Pat. No. 5, 661, 760; Col. 11, Lines 3-25 and Lines 57-62).

Regarding Claim 17, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claim 16. Patapoutian et al. further teaches wherein the servo circuit comprises: a sample circuit operable to generate samples of the servo signal (Pat. No. 5, 661, 760; See Abstract); and a Viterbi detector coupled to the sample circuit and operable to recover the servo data from the samples of the servo signal (Pat. No. 5, 661, 760; Col. 5, Line 64 to Col. 6, Line 13 and Abstract and Fig. 1).

Regarding Claim 18, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claim 16. Patapoutian et al. further teaches wherein the servo circuit comprises a decoder operable to decode the recovered servo data (Pat. No. 5, 661, 760; See Abstract. Patapoutian et al. teaches that the Viterbi detector also decodes the ¼ signal.).

Regarding Claim 19, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claim 16. Patapoutian et al. further teach wherein the read head comprises a read-write head (Pat. No. 5, 661, 760; Col. 5, Lines 15-21, Lines 28-32 and Lines 57-63 and Col. 12, Lines 1-12).

Regarding Claims 3 and 21, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claims 1 and 20, respectively. Patapoutian et al. further teach wherein the first, second, third, and fifth logic levels equal logic 0; and the fourth and sixth logic levels equal logic 1 (Pat. No. 5, 661, 760; Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that these logic levels can be achieved according to the configuration of zeros and ones that the disk drive enhances.).

Regarding Claim 22, Patapoutian et al. and Fredrickson et al. teach al the limitations of Claim 20. Patapoutian et al. further teaches wherein the coding comprises: coding the first logic level as a first group of four consecutive bits (Patapoulitian et al. teaches that each group of bits consists of 4 consecutive bits (Pat. No. 5, 661, 760; Col. 3, Lines 55-58. Patapoulitian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--"); and coding the fourth logic level as a second group of four consecutive bits (Patapoulitian et al. teaches that each group of bits consists of 4 consecutive bits (Patapoulitian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--").).

Regarding Claim 23, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claim 20. Patapoutian et al. further teach wherein the first and second portions of the first group and the first and second portions of the second group respectively comprise first and second halves of the first and second groups ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1")).

Regarding Claim 28, Patapoulitian et al. and Fredrickson et al. teach all the limitations of Claim 27. Patapoulitian et al. further teaches wherein: the first and second code symbols each comprise a number of code bits (Patapoulitian et al. teaches that each group of bits consists of 4 consecutive bits (Pat. No. 5, 661, 760; Col. 3, Lines 55-58). Patapoulitian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--".); and the lengths of the first and second code symbols are each less than the product of the number and a length of a servo-bit region (Patapoulitian et al. teaches that each group of bits consists of 4 consecutive bits (Patapoulitian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--").).

Regarding Claims 25, 26 and 29, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claims 24 and 27, respectively. Patapoutian et al. further teach wherein: the first bit equals a logic 0; and the second bit equals a logic 1 (Pat. No. 5, 661, 760; Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that these logic levels can be achieved according to the configuration of zeros and ones that the disk drive enhances.).

Regarding Claim 30, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claim 27. Patapoutian et al. further teaches wherein the first and second portions of the second code symbol are or are approximately half as long as the second code word ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1").).

Regarding Claim 31, Patapoutian et al. and Fredrickson et al. teach all the limitations of Claim 1. Fredrickson et al. further teach wherein the second group is non-palindromic (Pat. No. 6, 400, 288; Table 3, wherein Fredrickson et al. teach a binary sequence of 00001100, wherein one of the groups is palindromic ("0000") and the second group has a third logic level ("11") and a fourth logic level ("00").). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to generate binary sequences in order to reduce the occurrence of bit shift errors (Pat. No. 6, 400, 288; Col. 10, Lines 43-48).

Response to Arguments

Applicant's arguments filed 08/10/2004 have been fully considered but they are not persuasive.

In Claims 1, 4, 8, 10, 11, 14, 16, 20, 24, 27, 32 and 33, Applicant argues that Fredrickson does not teach wherein that the palindromic portion represents a logic levels. Examiner cannot concur with the Applicant because nowhere in the Applicant's Specification there is an actual clarification of the meaning of logic levels. Actually, the Examiner is assuming logic level to be as described in IEEE Standard Terms, which is the following: logic level: any level within one of two non-overlapping ranges of values of voltage used to represents logic states. In the digital field, these are represented with 0 and 1, as defined in the following, also given by the IEEE

Standard Terms: logic 0 and logic 1: logic voltage levels used for digital signals. Examiner finds that the word "palindromic" or any phrase inferring the code to be "palindromic" is not in the Applicant's Specification. Examiner exhorts the Applicant to clarify these definitions of "logic level" and "palindromic" as being claimed.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (703) 305-8411. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Hudspeth can be reached on (703) 308-4825. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gpr
01/26/2005.

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